Scalable Fabrication of Nanowire Photonic and Electronic Circuits Using Spin-on Glass

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ABSTRACT

We present a method which can be used for the mass-fabrication of nanowire photonic and electronic devices based on spin-on glass technology and on the photolithographic definition of independent electrical contacts to the top and the bottom of a nanowire. This method allows for the fabrication of nanowire devices in a reliable, fast, and low cost way, and it can be applied to nanowires with arbitrary cross section and doping type (p and n). We demonstrate this technique by fabricating single-nanowire p-Si(substrate)−n-ZnO(nanowire) heterojunction diodes, which show good rectification properties and, furthermore, which function as ultraviolet light-emitting diodes.

The field of semiconductor nanowires has witnessed rapid growth in recent years due to the development of inexpensive methods for their synthesis in large quantities. However, practical circuits necessitate the development of techniques for assembling nanowire devices in a highly parallel, scalable, and reproducible manner over large areas. Several studies have explored candidate methods to achieve this goal such as electric field-directed (dielectrophoresis),[1] fluidic,[2] and solution-based assembly methods.[3–5] These studies have explored the two complementary aspects needed for the development of large-scale integrated circuits. First, they illustrate methods to geometrically arrange nanowires over large areas, achieving some degree of control over nanowire-to-nanowire spacing and orientation. At the same time, they have also studied ways of fabricating electrical contacts to the nanowires thus aligned. However, all reports to date have focused exclusively on device geometries involving electrical contacts to opposite ends of nanowires along the axial direction[6] so that electrical current flows along the nanowire. This geometry may be used, for example, for the construction of field-effect transistors,[4] where the nanowire length forms the channel, or for p−n junctions formed along the axial direction of the nanowire. Such a geometry, however, presents limitations, especially in the case of single nanowire

p−n junctions because some materials are not amenable to doping of both types, most notably zinc oxide (ZnO).[7]

An alternative candidate geometry for the development of integrated nanowire circuits involves the fabrication of devices at the interface between nanowires and the underlying substrate (such as silicon). These junctions have been shown to result in p−n heterojunction diodes, which exhibit rectifying properties and, under certain conditions, also light emission.[8–12] The challenge in this particular geometry is the fabrication of top metallic contacts to the nanowires in a way that the contact does not short directly to the substrate.[9] Thus, this geometry requires a spacer layer that separates the substrate from the top contact on the sides of the nanowire but which is absent on top of it. As we have previously shown,[9] an effective strategy to accomplish this is to pattern an electron-beam resist on the sides of the nanowire, therefore turning the resist into an insulating epoxy but leaving the top surface of the nanowire exposed.[9–11] This method, however, required the use of high-resolution electron-beam lithography, which does not lend itself to large-scale fabrication. Here we demonstrate a method that allows for the realization of this nanowire/substrate geometry without the need for high-resolution electron-beam lithography so that it is possible to adapt it for the large-scale fabrication of electronic and photonic circuits.

Our technique relies on the use of hydrogen silsequioxane (HSQ), also known as "spin-on glass", as the spacer layer between the substrate and the top metallic contact. Because of its low dielectric constant ($\varepsilon = 2.9$ at 1 MHz) and good

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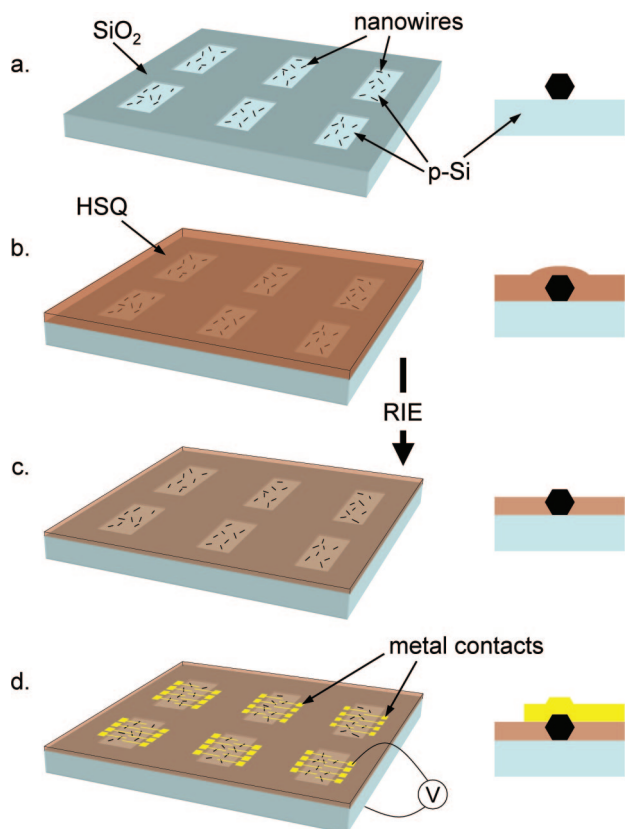§ Institute of Solid State Physics, University of Bremen.

Figure 1. Scalable method for the fabrication of nanowire/substrate photonic and electronic circuits. The schematics illustrate the key steps for the fabrication of p(substrate)−n(nanowire) heterojunction diodes, including (a) deposition of nanowires over the substrate, (b) spin-coating of HSQ, (c) RIE of HSQ in CF_4, and (d) deposition of a periodic metal electrode array using photolithography. The figures on the right show a detail of the process for an individual nanowire in cross section, whereas the figures on the left show an overall view of the procedure, emphasizing its scalability and parallelism.

planarization performance, HSQ has been the subject of intense research in recent years exploring its potential as interlayer dielectric material in high-density integrated circuits.[13,14] Compared with poly(methylmethacrylate) (PMMA), which was used as a negative electron-beam resist in previous work,[9–11] HSQ offers several properties that make it a more suitable alternative as spacer material: stability at high temperatures, etch resistivity, and significantly, it does not require high-dose electron-beam irradiation for cross-linking (which is the case for PMMA[9]). In fact, HSQ acquires sufficient mechanical integrity to withstand subsequent processing simply with a bake and curing procedure.

We illustrate the fabrication process of p(substrate)−n(nanowire) heterojunction diodes (Figure 1), using ZnO nanowires (see Experimental Methods). ZnO has a direct band gap energy of 3.37 eV at room temperature, which places its light-emission range in the ultraviolet (UV), and possesses several desirable properties for nanowire devices.[15–18] Its exciton binding energy of ∼60 meV provides an enhancement of the radiative transition rate, at room temperature, compared to the ∼25 meV exciton binding energy for GaN. However, despite the promise for improved light-emission properties, ZnO has lagged considerably in
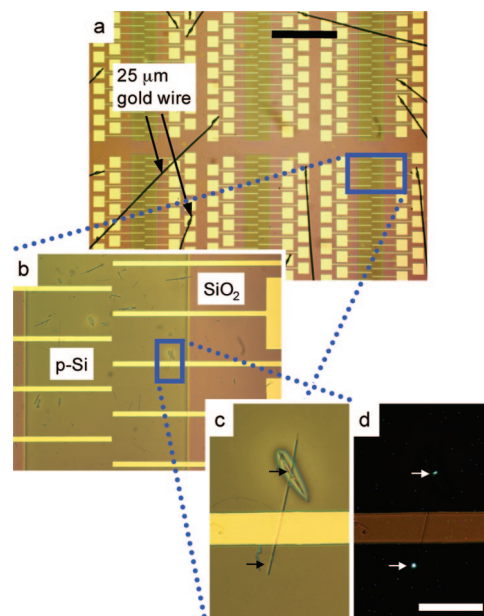

Figure 2. Optical micrographs of p-Si/SiO$_2$/n-ZnO heterojunction LEDs. (a), (b), and (c) show increasing levels of magnification. The 25 μm gold wires in (a) are leads for electrical contacts to individual pads. The scale bar in (a) is 1 mm. (d) Single-nanowire LED under a forward bias showing light emission, indicated by the arrows. The arrows in (c) point to the same location as in (d). The scale bar is 30 μm. A stray nanowire intercepts the LED on the upper part of (c) and (d). The oval feature surrounding the stray nanowire is due to the varying thickness of the HSQ film.

performance compared to the III-nitrides.[19] For example, there is no demonstration of large band edge-to-deep level emission ratio from electrically pumped ZnO nanowire light-emitting diodes (LEDs).[9,19–22] Remarkably, this problem has even been ubiquitous in thin-film-based ZnO LEDs.[7] *Here we demonstrate that our p−n heterojunction diodes do, under certain conditions, show dominant UV emission.*

The fabrication procedure starts with a heavily doped p-type silicon (p-Si) substrate (see Experimental Methods). Nanowires of n-type conductivity are then randomly dispersed (Figure 1a). The contact area between the nanowires and the p-Si defines p−n heterojunctions as well as the bottom contact to the nanowires. HSQ is then spun onto the substrate, with a resulting profile as shown schematically for a single nanowire on the right part of Figure 1b. The figure shows that, because of the spinning process, the thickness of the film tends to be thinner on top of the nanowires than on the spaces between them *rather than providing conformal coverage.* This is the key point to proceed without the need for high-resolution lithography. Etching a controlled amount of HSQ therefore leads to the top surface of the nanowires becoming exposed but not the underlying p-Si substrate (Figure 1c and Supporting Information Figure 1). Finally, photolithography is used to define a periodic pattern of metallic leads to contact the nanowires (Figure 1d). In this demonstration, the nanowires were randomly dispersed onto the substrate, resulting in nanowires also being randomly contacted by the metallic leads (in many cases with one lead contacting several nanowires). Figure 2 shows optical micrographs of a completed wafer, which illustrate the key
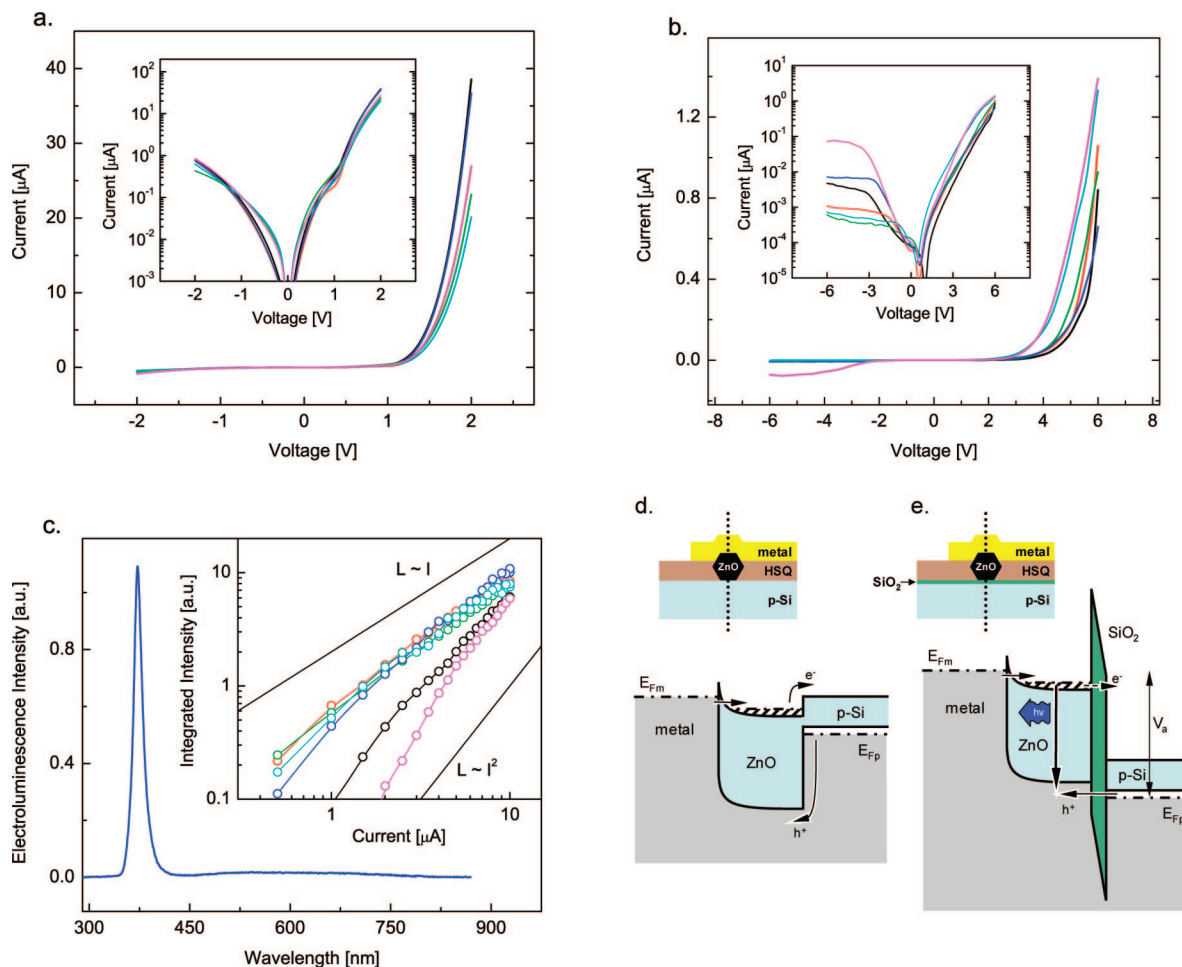
Figure 3. Room temperature characteristics of n-ZnO nanowire/p-Si substrate heterojunction diodes. Current−voltage characteristics for six devices (a) with no intervening oxide layer and (b) with a ∼7−8 nm SiO$_2$ insulating layer between the nanowire and the substrate. The insets show the same data in semilogarithmic scale. (c) Electroluminescence (EL) spectra from a n-ZnO nanowire/p-Si substrate heterojunction diode with a ∼7−8 nm SiO$_2$ insulating layer between the nanowire and the substrate and (inset) current dependence of the EL intensity for six different devices. Devices with no insulating layer showed no EL. Schematic band diagrams for a device (d) without and (e) with a SiO$_2$ thin film. The dotted lines indicate the plane along which the band diagrams are drawn.

features of the technique: (2a) arrays of devices with 125 μm electrode spacing repeated over an area of ∼4 × 8 mm^2, and (2c−e) individual ZnO nanowire LEDs connected to metallic leads. Interestingly, we have also observed efficient coupling between overlapping nanowires as evidenced by light emission from a nanowire, which crosses a nanowire LED (Supporting Information Figure 2).

We have observed dominant UV electroluminescence (EL) from individual ZnO nanowires, at room temperature, under moderate applied voltages (∼2E_g/e, where E_g is the band gap of ZnO). *An essential feature has been the introduction of a thin insulating film between the p-Si substrate and the n-ZnO nanowires. If the film is omitted, no electroluminescence is observed.* Figure 3 shows the current−voltage (I−V) characteristics for several devices made with our technique. Figure 3a corresponds to six devices where the insulating SiO$_2$ film is omitted. In this case, the p-Si substrate is treated with a buffered hydrofluoric acid solution immediately before deposition of the nanowires to ensure the removal of any residual native oxide. The I−V curves show good rectification and reproducibility, with current levels ∼40 μA at 2 V. No UV EL has been observed for these devices for currents up

to 1 mA. In contrast, Figure 3b shows the I−V curves corresponding to six devices where a thin (∼7−8 nm) SiO$_2$ film was applied to the p-Si substrate before depositing the nanowires (see Experimental Methods). The I−V curves also show good rectification properties, but the current levels are significantly reduced compared to the devices with no insulating film (∼1 μA at 6 V). UV EL was observed in each device tested. The EL spectrum (Figure 3c) peaks near the band gap of ZnO and is in excellent agreement with the PL spectrum (Supporting Information Figure 3). Note that there is negligible deep-level emission, unlike previous reports of ZnO LEDs. The inset in Figure 3c shows the light−current curves corresponding to six devices, the majority of which exhibit nearly linear behavior at higher current.

These results can be understood with the band diagrams shown in Figure 3d,e. The omission of the insulating layer results in a band diagram as shown in Figure 3d.[21] In that case, the barrier for hole injection into ZnO is approximately 2.5 eV but remains essentially constant with applied voltage, therefore making it impossible for hole injection to occur. Thus no light is produced. On the other hand, if an

intervening dielectric layer is present (Figure 3e), sufficient potential energy difference could be maintained between the two semiconductors to make tunneling of electrons from the valence band of ZnO into p-Si energetically possible, which is equivalent to hole injection in the opposite direction. This results in UV light emission. A similar mechanism for UV light emission was recently observed in n-GaN nanowire/p-Si substrate heterojunction diodes,[10,11] where the role of the tunnel barrier was attributed to a combination of the p-Si native oxide as well as a native oxide shell surrounding the GaN nanowires.

This work demonstrates a simple yet powerful technique to independently contact the top and bottom of single nanowires. Our approach is intrinsically scalable because every step involved can be carried out in parallel over an entire wafer. We have shown that our method results in good p−n heterojunctions when applied to ZnO nanowires on a p-Si substrate. Furthermore, we have proven the key importance of an insulating layer for the generation of EL in this geometry.

It is important to note that the method presented here is *independent* of the geometrical arrangement of the dispersed nanowires and can therefore be combined with an appropriate nanowire alignment strategy[1–5] to significantly expand its range of applications. For example, a promising approach to organize nanowires over large areas makes use of the Langmuir−Blodgett technique.[3,4] In this method, nanowires are spread onto the surface of the aqueous phase in a Langmuir−Blodgett trough and compressed, which causes the nanowires to become aligned along their long axes. This process allows for the accurate control of the average separation between nanowires simply by means of the degree of compression. Furthermore, the transfer of aligned nanowires is carried out by simply bringing a substrate into contact with the nanowire suspension, which is compatible with our method. To conclude, we believe that the combination of the new fabrication method demonstrated here with a nanowire alignment technique, such as the one just described, offers the possibility of unparalleled control over the large-scale fabrication of nanowire photonic and electronic circuits.

Experimental Methods. Nanowire Synthesis. Single-crystalline ZnO nanowires were synthesized in a horizontal tube furnace by a simple vapor transport technique.[23] Two grams of high-purity ZnO powder as source material were placed in an alumina boat and heated up to 1350 °C, allowing substantial evaporation. Silicon substrates covered with a 4 nm thin Au film were placed at the cooler end of the tube furnace at a temperature between 1050−1100 °C. The vapor was transported at a pressure of 100 mbar by Ar gas flow of 50 sccm to the substrates, initiating the catalytic driven vapor−liquid−solid (VLS) growth process[24] of the ZnO nanowires. After a growth time of 30 min, the as-deposited nanowires are typically up to 100 μm long and between 100−250 nm wide, as determined by scanning electron microscopy (SEM). Electron dispersive spectrometry (EDS) revealed only stoichiometric zinc and oxygen signals. Additional transmission electron microscope (TEM) and X-ray diffraction (XRD) investigations confirmed that the nanowires are of wurtzite structure and the *c*-axis is the growth direction.[23]

Device Fabrication. The fabrication procedure starts with a heavily doped p-type silicon (p-Si) substrate ($\sim10^{19}$ cm^{-3}) covered by a 200 nm thermal oxide layer. Photolithography and buffered hydrofluoric acid (BOE) are used to create an array of openings ($\sim400 \times 2100$ μm^2) through the thermal oxide, thereby exposing the underlying silicon. The nanowires (of n-type conductivity) are then transferred to the p-Si substrate by bringing the nanowire growth substrate into contact with the p-Si substrate. The nanowire growth substrate contains a "forest" of nanowires, so nanowires break off and attach to the p-Si substrate upon placing the nanowire substrate face down onto the p-Si substrate. This results in a random arrangement of nanowires in contact with the p-Si. For the fabrication of light-emitting diodes (see text), a thin film ($\sim7−8$ nm) of SiO$_2$ grown by plasma-enhanced chemical vapor deposition (PECVD) is deposited before transferring the nanowires.

HSQ (FOx-12 from Dow Corning) is then spun onto the p-Si with the nanowires (using a spin speed of 5000 rpm results in a film ~80 nm thick) and baked and cured in a hot plate at 100 °C for 1 min and 350 °C for 1 h. The HSQ film is then thinned down (by ~35 nm) by reactive ion etching (RIE) using CF$_4$ gas for 35 s (CF$_4$ gas flow of 5 sccm, H$_2$ gas flow of 4 sccm, 150 W of microwave power, and 50 W of RF power, at a process pressure of 10 mTorr). This exposes the top surfaces of the nanowires. Photolithography is then used to define a periodic pattern of leads, after which Ti(10 nm)/Au(100 nm) is deposited with an electron-beam evaporator. Without a preannealing step, this provides an ohmic contact to the ZnO nanowires.[25,26] It is important to note that in order to spin-coat the photoresist on the HSQ film, it is necessary to expose the thinned-down HSQ film to an oxygen plasma first. This forms a layer of SiO$_2$ on the HSQ,[27,28] which makes it resistant to the photoresist solvent.

Measurements. Current−voltage characteristics were measured with a Keithey 2400 source/meter. The electroluminescence setup consisted of a 36× reflective microscope objective with an aluminum coating, coupled to a 1/4 m spectrometer (150 lines mm^{-1} grating) and a thermoelectrically cooled CCD camera (InstaSpec IV 78437 open electrode).

Supporting Information Available: Scanning electron microscope image of the cross section of a nanowire, spin coated with HSQ, after the HSQ covering the top of the nanowire has been removed; optical micrograph of a p-Si/

SiO$_2$/n-ZnO heterojunction LED exhibiting efficient interwire optical coupling; photoluminescence spectrum of a single ZnO nanowire at room temperature. This material is available free of charge via the Internet at http://pubs.acs.org.

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